CLAIMS

What is claimed is:

1. A method of testing a core module comprising steps of:

(a) providing a core module of an integrated circuit design;

(b) connecting an end user input and a core module test input to separate I/O pins of the core module to isolate logic associated with an end user signal from that associated with a core module test signal; and

(c) multiplexing the end user signal and the core module test signal in the core module in response to a core module test mode signal.

2. The method of Claim 1 wherein the core module test signal is a synchronous or asynchronous signal.

3. The method of Claim 1 wherein the core module test signal is a static signal.

4. The method of Claim 3 wherein the core module test signal is a set or reset signal.

5. The method of Claim 3 further comprising a step of switching power to the core module between an on

state and an off state in response to the core module test signal.

6. The method of Claim 1 wherein the core module test signal is a synchronous or asynchronous signal.

7. The method of Claim 1 wherein step (b) further comprises connecting a core module scan test clock input to a separate I/O pin of the core module to isolate logic associated with the end user signal and logic associated with the core module test signal from logic associated with a core module scan test clock signal.

8. The method of Claim 7 wherein step (b) further comprises multiplexing the core module scan test clock signal in the core module in response to a core module scan test mode signal.

9. The method of Claim 8 wherein the core module test mode signal and the core module scan test mode signal are independent of each other.

10. The method of Claim 1 wherein step (b) comprises merging the I/O pin of the core module that is connected to the core module test input with an I/O pin at a top level of the integrated circuit design.

11. An apparatus comprising:

a core module of an integrated circuit;

an end user input and a core module test input connected to separate I/O pins of the core module to isolate logic associated with an end user signal from that associated with a core module test signal; and

a multiplexer for multiplexing the end user signal and the core module test signal in the core module in response to a core module test mode signal.

12. The apparatus of Claim 11 wherein the core module test signal is a synchronous or asynchronous signal.

13. The apparatus of Claim 11 wherein the core module test signal is a static signal.

14. The apparatus of Claim 13 further comprising a controller coupled to the core module for generating the static signal.

15. The apparatus of Claim 13 wherein the controller is a test access port controller.

16. The apparatus of Claim 11 wherein the core module test signal is a set signal, a reset signal, or a power on/off signal.

17. The apparatus of Claim 11 further comprising a core module scan test clock input connected to a separate I/O pin of the core module to isolate logic associated with the end user signal and logic associated with the core module test signal from logic associated with a core module scan test clock signal.

18. The apparatus of Claim 17 further comprising a multiplexer for multiplexing the core module scan test clock signal in the core module in response to a core module scan test mode signal.

19. The apparatus of Claim 18 wherein the core module test mode signal and the core module scan test mode signal are independent of each other.

20. The apparatus of Claim 11 wherein the I/O pin of the core module that is connected to the core module test input is merged with an I/O pin at a top level of the integrated circuit design.